1. (Twice Amended) A semiconductor structure, comprising:

a substrate;

a patterned oxide layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned oxide layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass;

a planarized layer of plasma-enhanced tetraethyl orthosilicate over at least a portion of the layer of the borophosphorous silicate glass, and not overlaying at least a portion of the borophosphorous silicate glass layer; and

a layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with at least a portion of the borophosphorous silicate glass region, the layers of the undoped silicate glass, borophosphorous silicate glass, planarized plasma-enhanced tetraethyl orthosilicate and second plasma-enhanced tetraethyl orthosilicate layer together forming a pre-metal dielectric stack.

2. The structure of claim 1 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2k and 8k angstroms.

3. (Amended) The structure of claim 1 wherein the second layer of plasma-enhanced tetraethyl orthosilicate is planar.

4. (Twice Amended) The structure of claim 3 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than approximately 15k angstroms.

6. (Twice Amended) An integrated circuit, comprising:

a substrate;

a dielectric layer disposed on the substrate;

a layer of undoped silicate glass disposed on the dielectric layer;

an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass;

a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, the planar dielectric layer directly overlaying at least a portion of the borophosphorous silicate glass and leaving exposed so as to not directly overlay at least a portion of the borophosphorous silicate glass; and

a dielectric layer disposed on the planar dielectric layer and the portions of the borophosphorous silicate glass which are not overlaid by the planar dielectric layer, the layers of undoped silicate glass, borophosphorous silicate glass, [and] planar dielectric layer, and a second dielectric layer together composing a pre-metal dielectric stack.

7. The integrated circuit of claim 6 wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

9. (Amended) The integrated circuit of claim 6 wherein the second dielectric layer is tetraethyl orthosilicate

10. (Amended) The integrated circuit of claim 6 wherein the second dielectric layer is plasma-enhanced tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

20. (Amended) A semiconductor device sub-structure, comprising:

a substrate;

an oxide layer disposed over the substrate in a pattern having a physical contour of at least one or more recessed portions and at least one or more extended portions;

a layer of undoped silicate glass disposed over the patterned oxide layer and having a physical contour of recessed and extended portions corresponding to the physical contour of the oxide layer;

a layer of doped silicate glass over the layer of undoped silicate glass and having a physical contour of recessed and extended portions corresponding to the physical contour of the layer of undoped silicate glass;

a first substantially planar layer of dielectric material covering at least one or more of the recessed portions of the layer of the doped silicate glass, and exposing at least one or more of the extended portions of the layer of the doped silicate glass layer; and

a second layer of dielectric material covering the first substantially planar layer of dielectric material and being in direct contact with the at least one or more extended portions of the layer of the doped silicate glass layer.

22. The device of claim 21 wherein the layer of doped silicate glass is a layer of borophosphorous silicate glass.

23. The device of claim 22 wherein the first layer of dielectric material is a layer of plasma-enhanced tetraethyl orthosilicate.

24. The device of claim 23 wherein the second layer of dielectric material is a layer of plasma-enhanced tetraethyl orthosilicate.

25. The device of claim 24 wherein the second layer of dielectric material is substantially planar.

26. The device of claim 25 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2k and 8k angstroms.

27. The device of claim 26 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than approximately 15k angstroms.